AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A data processing apparatus for determining a quantization scale ~~of the quantization~~ when quantizing and encoding processed data, the data processing apparatus comprising:

a specifying circuit for specifying a bit rate ~~by which~~ used to provide encoded data ~~is supplied~~ for decoding, [[at]] the ~~time of decoding~~ bit rate being based on encoding of the encoded data ~~obtained by the encoding;~~

an encoding difficulty detection circuit for detecting [[the]] encoding difficulty ~~of encoding~~ of [[the]] processed data that is encoded; [[and]]

a quantization control circuit for controlling the quantization scale based on the bit rate ~~specified by the specifying circuit~~ and the encoding difficulty ~~detected by the encoding difficulty detection circuit;~~

an indicator generation circuit for generating, based on the encoded data, indicator data specifying an amount of stored data of a storage circuit provided at a decoding side, the storage circuit storing and supplying the encoded data for decoding; and

a target calculation circuit for calculating a target bit rate indicating a target value of the bit rate based on the indicator data, wherein the quantization control circuit controls the quantization scale to cause the bit rate to approach a value based on the target bit rate.

2. (Currently Amended) A data processing apparatus as set forth in claim 1, wherein [[saod]] the quantization control circuit controls [[said]] the quantization scale ~~so as to make said quantization scale smaller the higher said~~ in relation to the detected encoding difficulty ~~detected by said encoding difficulty detection circuit~~.

3. (Cancelled)

4. (Currently Amended) A data processing apparatus as set forth in claim [[3]] 1, wherein [[said]] the target calculation circuit calculates [[said]] the target bit rate based on a difference between a designated final target bit rate and an average bit rate of past encoded data ~~so that said difference becomes small~~.

5. (Currently Amended) A data processing apparatus as set forth in claim 4, wherein [[said]] the target calculation circuit calculates [[said]] the target bit rate ~~so as~~ to avoid [[said]] underflowing the storage circuit ~~underflowing~~.

6. (Currently Amended) A data processing apparatus as set forth in claim 3, wherein [[said]] the target calculation circuit calculates [[said]] the target bit rate ~~so as~~ to avoid [[said]] underflowing the storage circuit ~~underflowing~~.

7. (Currently Amended) A data processing apparatus as set forth in claim 3, wherein [[said]] the specification circuit specifies [[said]] the bit rate of [[said]] the encoded data read from [[said]] the storage circuit ~~for supply~~ and supplied for decoding at [[said]] the

decoding side.

8. (Currently Amended) A data processing apparatus as set forth in claim 7, wherein [[said]] the specification circuit specifies [[a]] the bit rate ~~of said encoded data~~ based on an average amount of bits of pictures in past encoded data and a picture rate of [[said]] the pictures.

9. (Currently Amended) A data processing apparatus as set forth in claim 1, wherein when [[said]] the encoded data is comprised of a plurality of pictures, [[said]] the quantization control circuit controls [[said]] the quantization scale ~~of said~~ for the plurality of pictures.

10. (Currently Amended) A data processing apparatus as set forth in claim [[3]] 1, wherein [[said]] the quantization control circuit determines a new quantization scale and ~~performs the above control~~ controls the new quantization based on a ratio between [[said]] the bit rate, the ~~specified by said specification circuit and said~~ target bit rate ~~calculated by said target calculation circuit~~, and the previously determined quantization scale.

11. (Currently Amended) A data processing apparatus as set forth in claim [[3]] 1, wherein [[said]] the quantization control circuit determines a new quantization scale and ~~performs the above control~~ controls the new quantization based on ~~a difference between said~~ the bit rate, the ~~specified by said specification circuit and said~~ target bit

rate ~~calculated by said target calculation circuit~~ , and [[on]] the previously determined quantization scale ~~so as~~ to suppress overshooting and undershooting of [[said]] the bit rate.

12. (Cancelled)

13. (Currently Amended) An encoding device ~~having~~ for determining a quantization scale when quantizing and encoding processed data, the encoding device comprising:

a quantization scale calculation circuit for calculating the quantization scale[[,]];

a quantization circuit for quantizing the processed data based on the quantization scale ~~calculated by the quantization scale calculation circuit~~[[,]]; and

an encoding circuit for generating [[the]] encoded data by encoding [[the]] a quantization result [[of]] generated by the quantization circuit, wherein the quantization scale calculation circuit ~~comprising~~ comprises:

a specifying circuit for specifying a bit rate ~~by which~~ used to provide encoded data ~~is supplied~~ for decoding, [[at]] the ~~time of decoding~~ bit rate being based on encoding of the encoded data ~~generated by the encoding circuit~~;

an encoding difficulty detection circuit for detecting an encoding difficulty of [[the]] processed data that is encoded~~, and~~;

a quantization control circuit for controlling the quantization scale based on the bit rate ~~specified by the specifying circuit~~ and the encoding difficulty ~~detected by the encoding difficulty detection circuit~~;

an indicator generation circuit for generating, based on the encoded data, indicator data specifying an amount of stored data of a storage circuit provided at a decoding side, the storage circuit storing and supplying the encoded data for decoding; and

a target calculation circuit for calculating a target bit rate indicating a target value of the bit rate based on the indicator data, wherein the quantization control circuit controls the quantization scale to cause the bit rate to approach a value based on the target bit rate.

14. (New) A data processing method for determining a quantization scale when quantizing and encoding processed data, the data processing method being executed by an encoding device and comprising:

specifying a bit rate used to provide encoded data for decoding, the bit rate being based on encoding of the encoded data;

detecting encoding difficulty of processed data that is encoded;

controlling the quantization scale based on the bit rate and the encoding difficulty;

generating, by using an indicator generation circuit in the encoding device, indicator data specifying an amount of stored data of a storage circuit provided at a decoding side, the amount being based on the encoded data stored in the storage circuit to be supplied for decoding; and

calculating, by using the encoding device, a target bit rate indicating a target value of the bit rate based on the indicator data, wherein the quantization scale is controlled to cause the bit rate to approach a value based on the target bit rate.